AMENDMENTS TO THE CLAIMS

1. (Withdrawn) A method for delay compensation, comprising:

obtaining a clock signal used to generate a transmit clock;

counting clock cycles to provide a count signal associated with external device latency; and

capturing the count signal responsive to the clock signal.

2. (Withdrawn) The method, according to claim 1, wherein the count signal is captured with a register that approximates delay of an output driver stage.

3. (Withdrawn) The method, according to claim 2, wherein the output driver staged is clocked responsive to the clock signal.

4. (Withdrawn) The method, according to claim 1, further comprising:

obtaining an external read clock signal;

transmitting the count signal; and

capturing the count signal transmitted responsive to the read clock signal.

5. (Withdrawn) The method, according to claim 4, wherein the count signal is captured with a register that approximates delay of an input driver stage.

6. (Withdrawn) The method, according to claim 5, wherein the input driver staged is clocked responsive to the read clock signal.

7. (Withdrawn) The method, according to claim 6, wherein the count signal is externally looped back for the capturing responsive to the read clock signal.

8. (Currently Amended) A delay compensation system, comprising:

a first integrated circuit, the first integrated circuit including output drivers, one of the output drivers configured to provide a transmit clock signal and another of the output drivers configured to provide a read command signal; and

a second integrated circuit coupled to the first integrated circuit to receive the transmit clock signal and the read command signal, the second integrated

circuit configured to provide a read clock signal responsive to the transmit clock signal and to provide a data signal responsive to the read command signal[[;]], wherein the first integrated circuit includinges a delay compensation circuit, the delay compensation circuit being configured to operate synchronously with the transmit clock signal for a send portion and to operate synchronously with the read clock signal on a receive portion and wherein the delay compensation circuit includes a counter configured to count responsive to clock pulses to track latency of the second integrated circuit and wherein the counter is configured to reset a count responsive to a latency parameter of the second integrated circuit, the count being enabled to wait for a period of data validity for the data signal.

Claim 9. (Cancelled)

10. (Currently Amended) The system, according to claim 8 [[9]], wherein the send portion and the receive portion are coupled to one another via a loopback trace.

11. (Currently Amended) The system, according to claim 10 [[9]], wherein the first integrated circuit and the second integrated circuit are mounted to a printed circuit board having traces coupling the first integrated circuit to the second integrated circuit, the loopback track configured to approximate propagation delay associated with either the transmit clock signal or the read command signal and with either the read clock signal or the data signal along a portion of the traces.

12. (Currently Amended) The system, according to claim 11, wherein the counter is configured to count down to zero starting from the latency parameter of the second integrated circuit prior to resetting ~~send portion and the receive portion are coupled to one another via a loopback trace of the traces~~.

13. (Original) The system, according to claim 12, wherein the first integrated circuit is a field programmable gate array.

14. (Original) The system, according to claim 12, wherein the second integrated circuit is a memory.

15. (Currently Amended) The system, according to claim 8 [[9]], wherein the transmit clock signal is generated using a first clock signal, and wherein the read command signal is generated using a second clock signal.

16. (Original) The system, according to claim 15, wherein the first clock signal is used to clock the send portion.

17. (Original) The system, according to claim 15, wherein the first clock signal, the second clock signal and the clock pulses are separate signals from a same clock source.

18. (Original) The system, according to claim 17, wherein the clock source is a digital clock module.

19. (Original) The system, according to claim 15, wherein the first clock signal is a phase-shifted version of the second clock signal.

20. (Currently Amended) The system, according to claim 8 [[9]], wherein the first integrated circuit comprises at least one storage device coupled to receive a write enable signal, the write enable signal provided ~~enabled~~ responsive to output of the receive portion.

21. (Withdrawn) In an integrated circuit, a circuit for providing a data valid signal, comprising:

a counter for counting down latency associated with another integrated circuit;

a first register coupled to receive output of the counter at a first data input, the first register clocked synchronously with a transmit clock signal for the other integrated circuit to provide output of the counter at a first data output; and

a second register having a second data input coupled to the first data output of the first register to receive output of the counter, the second register clock synchronously with a read clock signal, the second register providing the valid data signal at a second data output.

22. (Withdrawn) The circuit, according to claim 21, wherein the first data output is coupled to the second data output via a loopback trace.

23. (Withdrawn) The circuit, according to claim 22, wherein the loopback trace is internal to the integrated circuit.

24. (Withdrawn) The circuit, according to claim 22, wherein the loopback trace is external to the integrated circuit.

25. (Withdrawn) The circuit, according to claim 22, wherein the loopback trace approximates propagation delay of the transmit clock signal from the integrated circuit to the other integrated circuit and of the read clock signal from the other integrated circuit to the integrated circuit.